Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A MOS transistor formed in a silicon substrate comprising: an active area surrounded by an insulating wall;

a first conductive strip covering a central strip of the active area;

a second conductive strip placed in the active area right below the first conductive strip; and

conductive regions placed in two recesses of the insulating wall and placed against ends of the first and second conductive strips, wherein, the silicon surfaces of the active area opposite to the conductive strips and conductive regions are covered with an insulator forming a gate oxide.

2. (Original) The transistor of claim 1 wherein the first and second conductive strips are made of polysilicon and the insulating wall is made of silicon oxide.

3. (Original) The transistor of claim 1 with two conductive strips, wherein the conductive regions placed against the first and second strips are separate.

4-8. (Canceled)

9. (Original) The MOS transistor of claim 1 wherein the second conductive strip is one of a plurality of second conductive strips, said second conductive strips together with said first conductive strips forming a stack.

10. (Original) The MOS transistor of claim 9 wherein the number of second conductive strips is 1, 2 or 3.

11. (Original) The MOS transistor of claim 10 wherein each said conductive strip of said stack is separated from one another by a silicon layer.

12. (Original) A MOS transistor formed in a silicon substrate comprising:

an active area surrounded by an insulating wall;

first conductive strip covering a central strip of the active area and forming first gate;

a first insulating layer immediately below said first conductive strip;

a second conductive strip placed in the active area below said first insulating layer and separated therefrom by a single-crystal silicon layer; and

conductive regions below first insulating layer, said conductive regions being placed in two recesses of the insulating wall and against ends of the second conductive strips and said silicon layer, said conductive regions and said second conductive strip forming second gate, wherein, the silicon surfaces of said active area facing said second conductive strip and conductive regions are covered with a second insulating layer.

~~12~~13. (Currently Amended) The MOS transistor of claim 11 wherein said first conductive strip is made of polysilicon.

~~13~~14. (Currently Amended) The MOS transistor of claim 11 wherein said first conductive strip is made of aluminum.

~~14~~15. (Currently Amended) The MOS transistor of claim 11 wherein said second conductive strip and said conductive regions are made of polysilicon.

~~15~~16. (Currently Amended) The MOS transistor of claim 11 wherein said first and second insulating layers are silicon oxide.

17. (New) The MOS transistor of claim 12 wherein the second conductive strip is one of a plurality of second conductive strips, said second conductive strips together with said first conductive strips forming a stack.

18. (New) The MOS transistor of claim 17 wherein the number of the plurality of second conductive strips is 2 or 3.

19. (New) The MOS transistor of claim 10 wherein each said conductive strip of said stack is separated from one another by a silicon layer.

20. (New) A MOS transistor comprising:

a substrate having an active area surrounded by insulating walls protruding from a surface of the substrate;

a stack of a plurality of layer pairs formed in the active area, each layer pair including a conductive layer and a single crystal silicon layer, the conductive layers alternating with the single crystal silicon layers;

an insulating layer overlying the stack;

a first gate overlying the insulating layer; and

a second gate comprising a first conductive region, a second conductive region and the plurality of the conductive layers of the stack, said first and second conductive regions respectively being against two opposing sides of the stack.

21. (New) The MOS transistor of claim 20 wherein the stack comprising three layer pairs of alternating conductive layers and single crystal silicon layers.

22. (New) The MOS transistor of claim 20 wherein the first gate is a polysilicon layer.

23. (New) The MOS transistor of claim 20 wherein the first gate is an aluminum layer.

24. (New) The MOS transistor of claim 20 wherein the second gate is made of polysilicon.